In the Claims

CLAIMS

Claims 1-37 (Canceled).

38. (Previously presented) Integrated circuitry comprising a semiconductor substrate having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising an oxide having nitrogen atoms therein, and the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location wherein the one elevational location is spaced from the gate, the gate dielectric layer of the n-type field effect transistors being different in composition from the gate dielectric layer of the p-type field effect transistors.

39. (Previously presented) The integrated circuitry of claim 38 wherein the gate dielectric layer of the p-type transistors comprises silicon dioxide.

40. (Previously presented) The integrated circuitry of claim 38 wherein the gate dielectric layer of the p-type transistors are of a different thickness relative the gate dielectric layer of the n-type transistors.

41. (Previously presented) The integrated circuitry of claim 38 wherein the concentration of nitrogen atoms in the gate dielectric layer of the p-type transistors at the one elevational location is from 0.1% molar to 10.0% molar.

42. (Previously presented) The integrated circuitry of claim 38 wherein the one elevational location is located proximate an interface of the gate dielectric layer with the semiconductor substrate.

43. (Previously presented) Integrated circuitry comprising a semiconductor substrate having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising silicon dioxide having nitrogen atoms therein, the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location and at a concentration of from 0.1% molar to 10.0% molar, the gate dielectric layer of the n-type field effect transistors comprising silicon dioxide material proximate an interface of the gate dielectric layer with the semiconductor substrate which is substantially void of nitrogen atoms.

44. (Previously presented) The integrated circuitry of claim 43 wherein the one elevational location is located proximate an interface of the gate dielectric layer with the semiconductor substrate.

45. (Previously presented) Integrated circuitry comprising a semiconductor substrate substantially void of nitrogen atoms and having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising an oxide having nitrogen atoms therein, the gate dielectric layer of the n-type field effect transistors being different in composition from the gate dielectric layer of the p-type field effect transistors, and the gate dielectric layer of the n-type field effect transistors comprising an interface with the gate wherein the composition proximate the interface is substantially void of nitrogen atoms.

46. (Previously presented) The integrated circuitry of claim 45 wherein the nitrogen atoms are higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location.

47. (Previously presented) Integrated circuitry comprising a semiconductor substrate substantially devoid of nitrogen atoms and having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising silicon dioxide having nitrogen atoms therein, the gate dielectric layer of the n-type field effect transistors comprising silicon dioxide material proximate an interface of the gate dielectric layer with the semiconductor substrate, the silicon dioxide material being substantially void of nitrogen atoms.

48. (Previously presented) The integrated circuitry of claim 47 wherein the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location.

49. (Previously presented) The integrated circuitry of claim 47 wherein the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location and at a concentration of from 0.1% molar to 10.0% molar.

50. (Previously presented) The integrated circuitry of claim 38 wherein the semiconductor substrate forms an interface with the respective n-type and p-type field effect transistors, and wherein the semiconductor substrate at the interface is substantially void of nitrogen atoms.

51. (Previously presented) The integrated circuitry of claim 43 wherein the semiconductor substrate at the interface is substantially void of nitrogen atoms.

52. (Previously presented) The integrated circuitry of claim 45 wherein the semiconductor substrate forms an interface with the respective n-type and p-type field effect transistors, and wherein the semiconductor substrate at the interface is substantially void of nitrogen atoms.

53. (Previously presented) The integrated circuitry of claim 47 wherein the semiconductor substrate at the interface is substantially void of nitrogen atoms.

54. (Previously presented) The integrated circuitry of claim 38 wherein the gate dielectric layer of the n-type transistors comprises an interface with the gate, and wherein the interface is substantially void of nitrogen atoms.

55. (Previously presented) The integrated circuitry of claim 38 wherein the gate dielectric layer of the n-type transistors is substantially void of nitrogen atoms.

56. (Previously presented) The integrated circuitry of claim 45 wherein the gate dielectric layer of the n-type transistors is substantially void of nitrogen atoms.

57. (Previously presented) The integrated circuitry of claim 45 wherein the gate dielectric layer of the p-type transistors comprises an interface with the gate, and wherein the interface is substantially void of nitrogen atoms.